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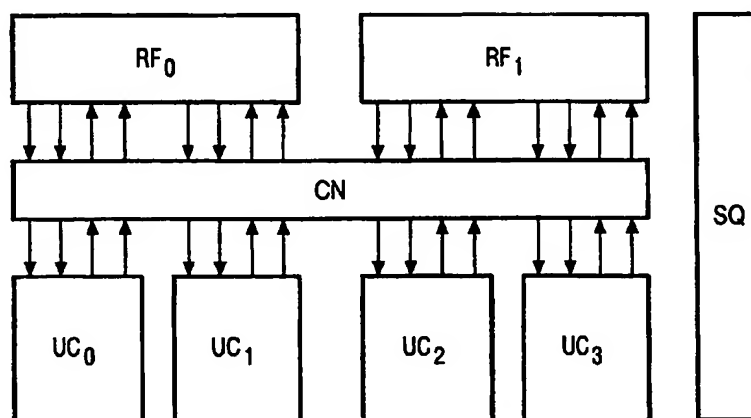
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(54) Title: MULTI-ISSUE PROCESSOR



(57) Abstract: A multi-issue processor comprises a plurality of issue slots (UC0, UC1, UC2 and UC3), each one of the plurality of issue slots having a plurality of functional units (FU0, FU1 and FU2) and a plurality of holdable registers (1 - 33 and 101 - 117). The plurality of issue slots comprises a first set of issue slots (UC1, UC2 and UC3) and a second set of issue slots (UC0), and the register file (RF0 and RF1) is accessible by the plurality of issue slots (UC0, UC1, UC2 and UC3). A location of at least a part of the plurality of holdable registers (1 - 33) in the first set of issue slots (UC1, UC2 and UC3) is different from a location of at least a corresponding part of the plurality of holdable registers (101 - 117) in the second set of issue slots (UC0). The holdable registers can prevent that the inputs of unused functional units change, which would result in unnecessary power dissipation. However, this increases the amount of state that has to be saved during interrupt handling. By varying the position of the holdable registers for different issue slots, less state saving may be required during interrupt handling, while maintaining a significant reduction in power consumption and improved performance.

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# INTERNATIONAL SEARCH REPORT

International Application No  
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**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 G06F9/38 G06F1/32

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 026 479 A (RAJE PRASAD A ET AL) 15 February 2000 (2000-02-15) column 3, line 53 - column 4, line 15 column 5, line 53 - column 6, line 47	1-3
A	US 5 452 401 A (LIN CHONG M) 19 September 1995 (1995-09-19) column 10, line 31 - line 43 -/--	1-3

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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- \* & \* document member of the same patent family

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	WU YE ET AL: "Power analysis of gated pipeline registers" ASIC/SOC CONFERENCE, 1999. PROCEEDINGS. TWELFTH ANNUAL IEEE INTERNATIONAL WASHINGTON, DC, USA 15-18 SEPT. 1999, PISCATAWAY, NJ, USA, IEEE, US, 15 September 1999 (1999-09-15), pages 281-285, XP010360298 ISBN: 0-7803-5632-2	

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